Nano Research
DOI 10.1007/s12274-014-0536-6
Research Article

ISSN 1998-0124
CN 11-5974/O4

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Nano Res., **Just Accepted Manuscript** • DOI: 10.1007/s12274-014-0536-6
http://www.thenanoresearch.com on July 3, 2014

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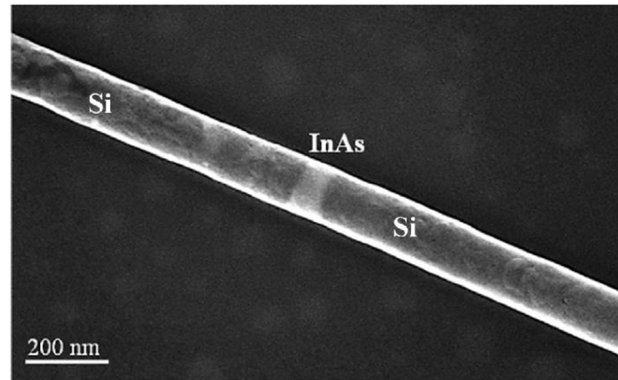

III-V/Si hetero-nanowire fabricated by liquid-phase epitaxy using ion beam implantation and millisecond range flash-lamp annealing. As an example, the InAs segments integrated into the Si NWs.

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DOI (automatically inserted by the publisher)
Review Article/Research Article **Please choose one**
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Received: day month year
Revised: day month year
Accepted: day month year (automatically inserted by the publisher)

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KEYWORDS

liquid phase epitaxy, InAs, heteronanowires, silicon, ion implantation

ABSTRACT

Direct integration of high-mobility III-V compound semiconductors with existing Si based CMOS processing platforms presents a main challenge to increase the CMOS performance and the scaling trend. Silicon hetero-nanowires with integrated III-V segments are one of the most promising candidates for advanced nano-optoelectronics as first demonstrated using molecular beam epitaxy techniques. Here we demonstrate a novel route for InAs/Si hybrid nanowire fabrication via millisecond range liquid-phase epitaxy regrowth using sequential ion beam implantation and flash-lamp annealing. We show that such highly mismatched systems can be monolithically integrated within a single nanowire. Optical and microstructural investigations confirm the high quality hetero-nanowire fabrication coupled with the formation of atomically sharp interface between Si and InAs segments. Such hybrid systems open new routes for future high-speed and multifunctional nanoelectronic devices on a single chip.

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Introduction

Quasi one-dimensional nanostructures like semiconductor nanowires (NWs) offer a great potential for future 3-D nanoelectronics [1-10]. In order to combine the well-established CMOS technology with the performance advantages of III-V semiconductors high quality III-V/Si heterojunctions have to be realized. Field-effect transistors [11-13], photodetectors [14], light-emitting diodes [15], gated resistors [8] and photovoltaic devices [16] have been fabricated using semiconducting nanowires. Recent progress in chemical vapour deposition CVD has allowed position-controlled integration of vertical III-V nanowires (NWs) [2, 17] or core-shell NW heterostructure on Si substrates [18]. In particular, the III-V compound semiconductors possess all required features for the next-generation high-speed logic applications. Most III-V binary semiconductors have a significantly higher electron mobility than Si and have a direct band gap which perfectly suits them for the optoelectronic devices. Among III-V semiconductors InAs has one of the highest electron mobilities which makes it an ideal candidate as the channel material for tunnel field effect transistors (TFET) operating at low voltage (< 0.5 V) without a loss of performance. The main obstacles facing towards the mass production of such hybrid systems are related to the difficulties of direct growth of III-V semiconductors on Si e.g. polar/non-polar surface incompatibility, large lattice mismatch and thermal expansion coefficients between III-V materials and Si. Previously, the ion beam implantation technique followed by flash-lamp annealing was used for the fabrication of Si/III-V heterojunctions in bulk silicon [19, 20] and SOI wafers [21]. Here we have studied the suitability of the ion beam implantation process for the silicon based axial hetero-nanowire formation. To this end, we processed samples with either [111] oriented as-grown Si NWs or NWs that were dispersed on an insulating Si wafer having a 100 nm SiO_2 top layer. These samples were implanted with In and As ions and subsequently annealed for 20 ms. Depending on the annealing temperature either the SiNW:InAsQD system or Si/InAs/Si heteronanowires with (111) oriented zinc blende InAs segments were fabricated. We have shown that the switching between the SiNW:InAsQD and the Si/InAs/Si system is due to the change of the recrystallization process during post-implantation annealing from the solid-phase epitaxial to the liquid-phase epitaxial (LPE) growth.

1. Experiments

The <111> oriented Si NWs were epitaxially grown on (100) Si substrates in an low-pressure chemical vapour deposition (LPCVD) system via the vapour-liquid-solid (VLS) growth mechanism using silane (SiH_4) as precursor gas and a thin (< 3 nm) magnetron sputtered Au layer as catalyst [22]. The diameter of the as-grown NWs is in the range of 50 to 200 nm. After NW growth the Au was removed with aqua regia. Basically two types of samples were investigated; as-grown, and planar Si NWs deposited on Si wafers having a 100 nm thermally grown SiO_2 layer. Before implantation the planar NWs were thermally oxidized by rapid thermal annealing to form a 20 nm SiO_2 shell. Both types of Si NWs were implanted with As and In ions with a fluence of 1, 2 or 3×10^{16} ion/cm^2 for each element. The ion implantation energy was chosen as 100 keV for As^+ and 140 keV for In^+ in order to form an overlapping depth distribution of In and As atoms within the Si NWs. After the implantation the samples were annealed at different temperatures utilising flash lamp annealing (FLA) system. The FLA was provided for 20 ms with preheating at 600 °C for 3 min [23]. The preheating was used to initialize the recrystallization of Si NWs and clustering of InAs. Since the preheating conditions were kept constant for all samples we will further refer to the FLA conditions only. The energy density deposited into the sample surface during FLA was in the range of 46 to 67 J/cm^2 corresponding to a final temperature in the range of 1000 – 1300 °C. The annealing was performed in continuous argon flow atmosphere. Moreover, selective-area ion beam implantation followed by FLA was performed on the planar Si NWs. To this end NWs were dispersed on an insulating Si substrate with 100 nm SiO_2 top layer. Two approaches were found to be suitable. The first approach was to deposit 120 nm SiO_2 by PECVD at 300 °C. With e-beam lithography implantation windows centred on NWs were patterned in a PMMA layer which acted as masking for the subsequent buffered HF etching to reveal the Si NW

core. Afterwards 54 nm SiO_2 were again deposited by PECVD resulting in an 174 nm oxide layer for implantation masking outside the implantation windows (Fig. 4a). For the second approach 50 nm SiO_2 was deposited by PECVD at 300°C. Subsequently a Ni hard mask was created by e-beam lithography, e-beam evaporation of 80 nm Ni and lift-off technique with acetone, leaving implantation windows of about 500 nm × 120 nm on the Ni-masked NWs.

The optical properties were investigated by micro-Raman spectroscopy. Back-scattering Raman spectroscopy was carried out on a WITec alpha300 confocal microscope setup with a Nd:YAG laser @532 nm equipped with a wide-aperture 100x objective. The micro-Raman spectra were recorded at room temperature in the range of 150 to 1000 cm^{-1} at low laser power of about 50 μW at the sample surface to prevent heating of the specimen. HRTEM, high-angle annular dark-field scanning TEM (HAADF-STEM), EDX and EELS were performed in cross-sectional geometry by means of an FEI TECNAI F20 operating at 200 keV. For the cross-section TEM investigation the lamellas were prepared along the axis of Si NW by focused ion beam milling.

2. Results and discussion

Figure 1 shows the SEM images of Si NWs implanted with different fluences and annealed at 58.1 J/cm² (a and b) and 66.5 J/cm² (c) or 54.2 J/cm² (d and e) for 20 ms. Due to the Z-contrast between Si and implanted elements, the InAs precipitates (bright area) are clearly seen in all NWs. The planar Si NWs annealed below the melting point of a-Si exhibit InAs nanodots randomly distributed over the whole length (see Fig. 1a and b). The size of the InAs nanodots increases with implantation fluence. In the case of samples implanted with a fluence of 3×10^{16} ions/cm² and annealed above the melting point of a-Si hybrid Si/InAs NWs with well separated InAs segments were formed (see Fig. 1c). The final temperature reached during FLA treatment strongly depends on the absorption coefficient of the annealed sample. Since as-grown samples with dense vertical Si NWs absorb much more light in the visible spectrum range than planar dispersed Si NWs, to obtain the same temperature the amount of energy deposited to the sample during FLA had to be increased.

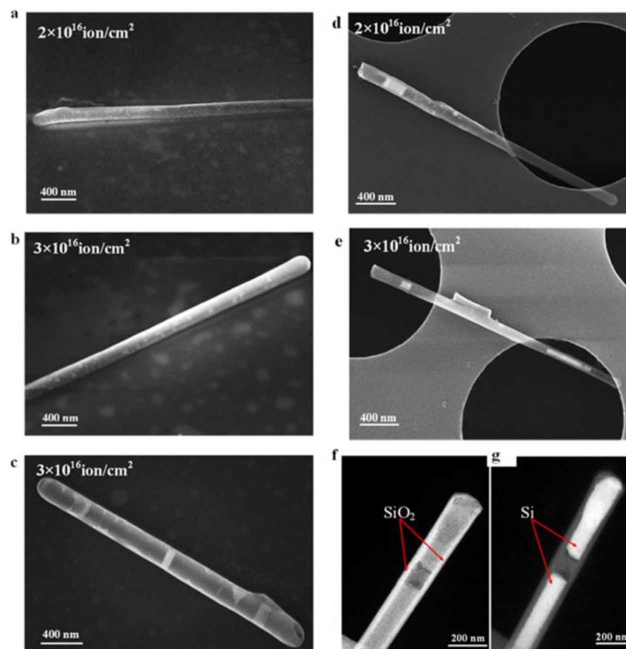

Figure 1. SEM images of planar deposited Si NWs (a-c), as-grown Si NWs (d and e) and EELS images (f and g) of the ion implanted and FLA treated Si NWs. NWs were annealed for 20 ms with an energy of 58.1 J/cm² (a and b), 66.5 J/cm² (c) and 54.2 J/cm² (d and e). (f) and (g) present EELS plasmon mapping of SiO_2 shell and Si plasmon mode, respectively, taken from the as-grown Si NW presented in (d). The ion fluencies are indicated in the images.

It turns out that the final temperature for the planar Si NWs annealed at 66.5 J/cm² for 20 ms is equivalent to 54.2 J/cm² for as-grown Si NWs, which corresponds to a peak temperature of about 1200 °C, whereas the maximum temperature reached in the planar Si NWs annealed at 58.1 J/cm² was lower by 100 °C. Immediately after high-fluence ion implantation the Si NWs are fully amorphous. Taking into account that the melting point of amorphous Si (a-Si) is about 200 ±50 K lower than in crystalline Si [24] and bulk InAs melts at about 940 °C we can assume that NWs presented in Figure 1c-e were molten during FLA. Hence the hybrid Si/InAs NW formation is due to millisecond range liquid-phase epitaxy. Operating in the liquid-phase regime, a giant diffusion of In and As takes place. During such process the amorphous-liquid/crystalline-solid interface moves along the NW with a velocity of 10-20 m/s floating the implanted elements together towards the ends of the Si NW where they segregate forming InAs segments (see Fig. 1c-e) [24]. Moreover, the diffusion coefficient for In and As in liquid Si (~10^{-4} cm²s⁻¹) is by about five

orders of magnitude larger than in the solid state [25]. This corresponds to the diffusion length L_D of implanted elements in the range of 2 μm/ms. The average length of investigated nanowires is about 2 μm, it means that the existence of liquid Si phase for 1 ms is sufficient to pass the whole length of nanowire by the implanted elements during FLA. In the case of samples annealed at 58.1 J/cm² (about 1100 °C) Si NWs are not molten and they recrystallize due to solid phase epitaxy (Fig. 1a). The formation of hybrid nanowires during millisecond range FLA treatment can be well described by explosive crystallisation process (ECP) [26, 27]. Geiler *et al.* proposed four types of ECP depending on the annealing parameters:(i) explosive solid-phase nucleation, (ii) explosive solid-phase epitaxy, (iii) explosive liquid-phase nucleation and (iv) explosive liquid-phase epitaxy [26]. The formation of the hybrid nanowires with well-defined InAs segments is the most probably due to explosive liquid-phase epitaxy in which LPE controls the crystallization process. Whereas, the recrystallization of the Si NWs with InAs QDs is governed by explosive solid-phase epitaxy. The investigated as-grown Si NWs were initially covered only with a native oxide. The electron energy-loss spectroscopy (EELS) plasmon mapping of Si and O taken after annealing exhibits the presence of a 25 nm thick shell oxide layer around the hybrid NW. Simultaneously Si is not present inside the InAs crystals, at least for the detection limit of our system (Fig. 1(g)). The SiO_2 shell spans the entire length of the Si NWs, even around the crystalline InAs segments (Fig. 1(f)). According to the simulation of the temperature distribution in Si NWs during 20 ms annealing the maximum temperature is reached after 17 ms. For the FLA at 54.2 J/cm² for 20 ms a temperature of 1000°C is reached after 10 ms, which is sufficient for the efficient oxide layer formation. We assume that before the Si NWs melts the silicon dioxide shell is formed consuming residual oxygen present in the annealing chamber. Based on our simulation the Si NWs are liquid for about 3 ms. The 25 nm thick shell oxide layer appears sufficient to stabilize the Si NW during explosive recrystallization. The temperature simulation was done based on the wave transfer matrix method for modelling the absorption of the flash light and the numerical solution of the one-dimensional heat equation [28]. The optical system taken into consideration for temperature simulation comprises the inert gas atmosphere of argon, amorphous Si NWs, the bulk Si and for planar NWs the 100 nm SiO_2 layer. The absorption of energy delivered to the sample during FLA process depends on the overall absorption and transmission of investigated system. The as-grown implanted SiNWs absorb about 97 % of incident flash lamp spectrum while the planar Si NWs absorb only 72 % of the light delivered to the sample surface. Therefore two different annealing parameters were used to obtain the same final temperature during FLA process. In further experiments it was observed that an SiO_2 shell is crucial for proper InAs crystallite formation, and 20-25 nm thick SiO_2 shells obtained by dry thermal oxidation as well as PECVD deposition were sufficient for the InAs recrystallization.

In addition, the microstructural properties and elemental composition of the hybrid Si/InAs NWs were investigated by high-resolution transmission electron microscopy (HRTEM) and energy-dispersive X-ray spectroscopy (EDX) spectroscopy, respectively. Figure 2(a) shows the HRTEM image of the atomically sharp interface between a Si NW and an InAs segment. The high-quality planar hybrid Si/InAs NWs are obtained only after high-fluence ion implantation (3×10^{16} ion/cm²) and millisecond range FLA treatment at the liquid-phase regime. For the smaller ion fluencies instead of the InAs segments the InAs QDs were formed. The EDX spectrum taken from the bright segment marked in Fig. 2(b) reveals mainly indium and arsenic with small oxygen and Si peaks (see Fig. 2(c)). The oxygen and silicon signals in the EDX spectrum are due to the NW's Si core and SiO_2 shell. The estimated concentration ratio from the EDX spectrum between indium and arsenic inside the InAs segment is 1:1. Also the TEM diffraction pattern confirms the formation of high-quality [111] oriented crystalline InAs segments visible as the blue spots in the inset of Fig. 2(b) while the red spots corresponds to the [111] oriented silicon nanowire. Differences in intensities and small irregularity for the [111] spots are caused by non-perfect crystallite-e-beam alignment during the measurements.

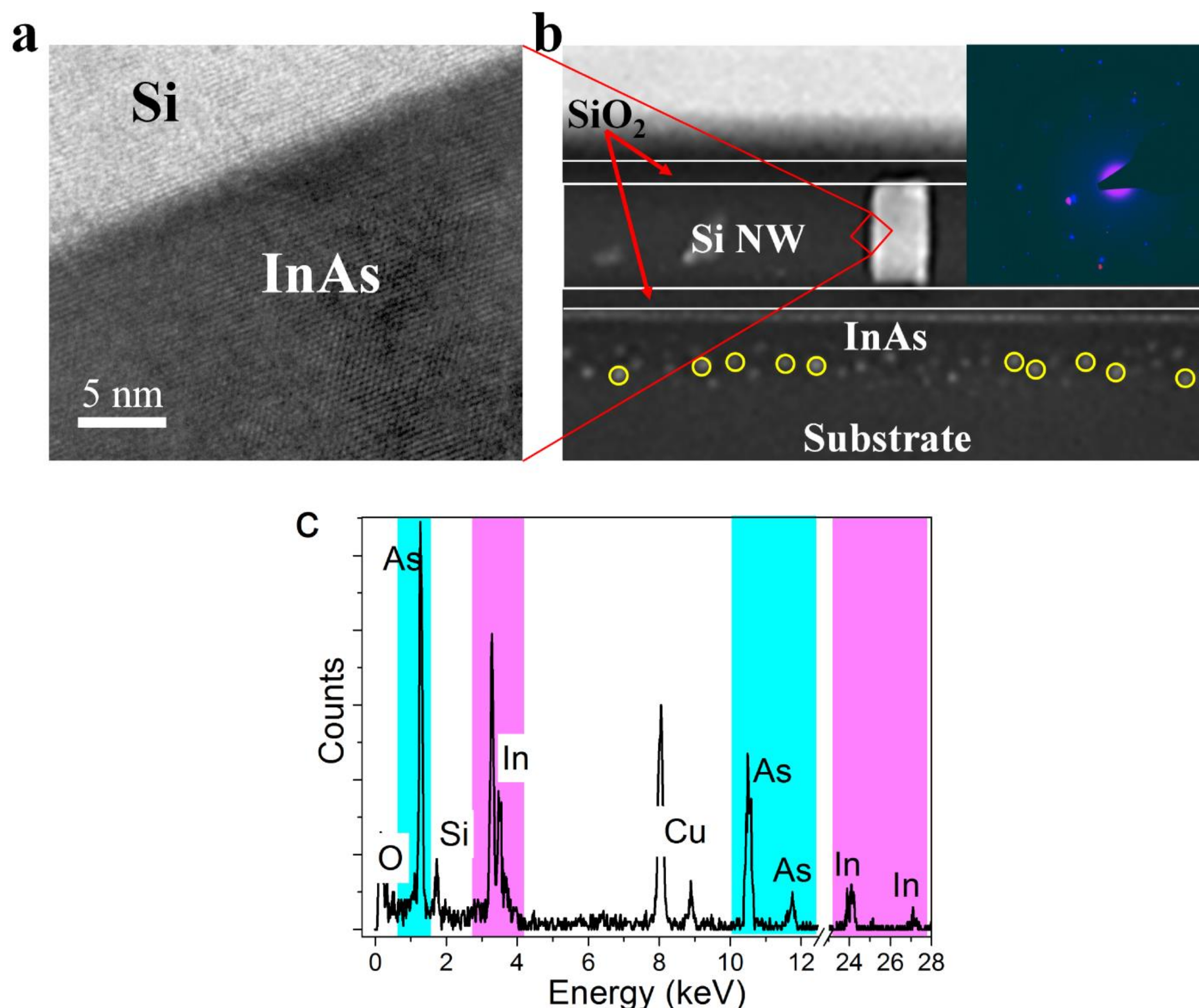

Figure 2. Planar Si/InAs hetero-nanowire. Bright field HRTEM micrographs of the interface between (111) Si and zinc blende (111) oriented InAs (a), Bragg contrast dark field TEM image of hybrid Si/InAs NW (b) and (c) shows EDX spectra taken from InAs segment visible in (b). The yellow circles below the nanowire pointed out InAs QDs in SiO_2 layer just below the NW. The inset in (b) shows the diffraction pattern obtained from the InAs crystal center. The blue spots corresponds to the zinc blende (111) oriented InAs crystal while the red spots are due to (111) oriented Si. Cu and O peaks in the EDX spectrum originate from the TEM specimen holder and SiO_2 shell.

The lattice parameter in [111] direction estimated from the diffraction pattern is 0.348 nm for InAs and 0.315 nm for silicon. This yields a relation of InAs/Si: 1.105, which is in good agreement to InAs/Si lattice mismatch of 11.6%. Besides InAs segments inside Si NWs small InAs nanodots are formed in the oxide layer around Si NWs (see Fig. 2(b)). They are formed around 70 nm below the surface which corresponds to the projected implantation range for In and As. The recrystallization process of Si NWs and formation of crystalline InAs segments were investigated by means of micro-Raman spectroscopy. Figure 3 shows the micro-Raman spectra obtained from a single hybrid Si/InAs NW. The micro-Raman spectrum recorded from the crystalline Si NW (curve 1 in Fig. 3) consists of a single peak located at 520 cm^{-1}, which corresponds to the longitudinal optical phonon mode in crystalline Si [29]. The Raman spectra obtained from regions containing InAs show two additional peaks at around 217 and 237 cm^{-1} due to transverse optical (TO) and longitudinal optical (LO) phonon modes in crystalline InAs (see curves 2 and 3 in Fig. 3). Because the lateral spatial resolution of our Raman system is larger than 400 nm while the length of the investigated InAs segment is typically about 150 nm, the Raman spectrum contains peaks corresponding to both crystalline InAs and Si.

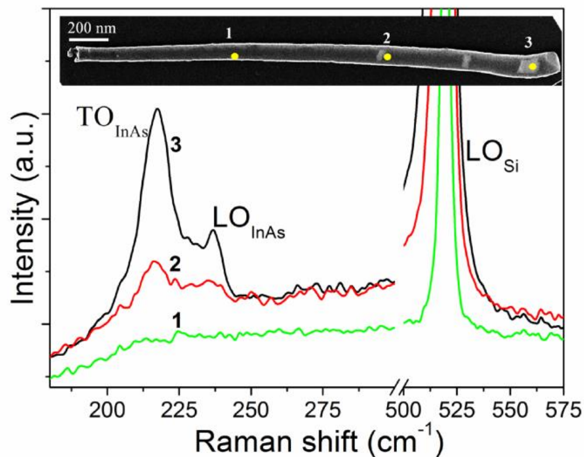

Figure 3. micro-Raman spectra of hybrid Si/InAs NWs taken at different positions along the NW. Spectra 2 and 3 are taken from crystalline InAs segments while spectrum 1 is taken from the part of nanowire without InAs. The inset shows the SEM image of the investigated NW with marked measurement points.

The peak positions of the InAs related TO and LO phonon modes fit well to the tabulated values for bulk InAs crystals [30]. This confirms the high quality of the InAs segment formation in Si NWs during FLA as well as material free of strain. Moreover, the TO phonon modes dominate the micro-Raman spectra indicating (111) orientation of InAs crystals inside Si NW, which is in good agreement with HRTEM data.

So far the InAs segments have random localization along the Si NW. In order to obtain InAs QDs at well-defined position, selective-area ion implantation was used. To this end, implantation windows were defined by e-beam lithography either using a 174 nm thick PECVD SiO_2 layer (Fig. 4(a)) or 50 nm thick Ni masks deposited over the Si NWs (Fig. 4(b)).

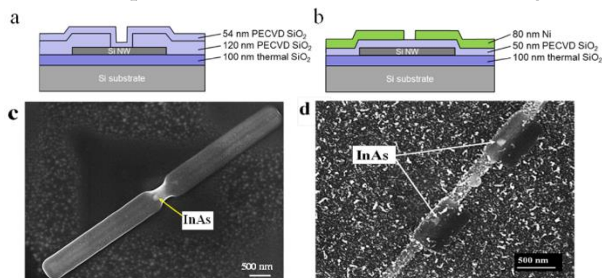

Figure 4. Schematics of sample cross-sections for selective area ion implantation (a and b) and corresponding SEM images of Si NWs with well localised InAs segments (c and d). The small flacks-like structure visible in (d) are from Ni mask processing.

Here the SiO_2 or Ni layer outside of the implantation window prevents doping and amorphization of the whole NWs. Prior to annealing the Ni layer was removed by HCl etching. Thus during the FLA step only the amorphized part of the Si NW is molten and the implanted In and As atoms are squeezed to the middle of the implanted area and the crystalline InAs segment is formed (see Fig. 4(c) and (d)). This is due to explosive liquid-phase recrystallization process which starts simultaneously from both sides of the implantation window. The size of InAs is determined by the diameter of Si NWs, area of the implantation window and the ion implantation fluence. Presented here, the InAs segment has the diameter of 120 nm (the same as implanted Si NW) and a length of about 60 nm, which means that in average the InAs crystals contain around 12×10^6 indium atoms. If we assume that all implanted indium (through a implantation window of 500 nm×120 nm) is accumulated inside the Si NW, the implanted part of the Si NW will contain around 16×10^6 indium atoms. Comparing now the number of implanted atoms with the number of atoms forming the InAs nanocrystal we can conclude that at least 75 % of implanted elements, both indium and arsenic, are agglomerated into single InAs segments. Taking into account the efficiency of the PECVD SiO_2 and Ni masking methods we can conclude that the SiO_2 layer is more stable against the ion implantation process. Ni layer was partially sputtered during ion implantation causing co-implantation of the top oxide layer below the Ni and the oxide shell around Si NW. This causes the surface roughening during chemical etching and FLA processes. Definitely the well control positioning of dispersed Si NWs on the CMOS circuits is a big challenge. Therefore in the next attempt the horizontal nanowires made on the SOI wafers utilising top-down approach will be explored. Such heterojunctions with well localised III-V segments hold great promise for future high performance 3D nanoelectronics.

3. Conclusions

We have demonstrated a novel route for the integration of III-V compound semiconductor material with CMOS technology. The presented method for the hetero-nanowire fabrication is based upon standard technologies commonly used in the microelectronic industry. The crystallographic orientation and shape of the InAs crystallites

embedded into Si NWs is fully controlled by the ion implantation and post-implantation annealing conditions. For a fixed ion fluence with increasing annealing temperature the ion implanted Si NWs are transformed from the SiNW:InAsQD system to Si/InAs/Si hetero-nanowires. The type of fabricated hybrid nanowires depends on the recrystallization process during post-implantation annealing. The Si/InAs/Si hybrid NWs obtained by the liquid-phase epitaxy show atomically sharp interfaces between Si and zinc blende InAs segments. Finally, the Si/InAs/Si hybrid NWs with well localised single InAs segments were fabricated using selective ion beam implantation. We have shown that the presented method can be used for both epitaxial and horizontal Si NWs. In the next step a pure top-down approach by appropriate e-beam patterning of Si or SOI wafers and dry etching, which can offer better more control of doping level, size and lateral distribution will be explored.

Acknowledgements

This work was partially supported by the Helmholtz-Gemeinschaft Deutscher Forschungs -zentren (HGF-VH-NG-713) and by the Austrian Science Fund (FWF) project No. I724-N16. The cleanroom facilities are provided by the Center for Micro- and Nanostructures (ZMNS) Vienna. Technical support by USTEM TU Wien is gratefully acknowledged.

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